IN THE CLAIMS:

Please amend claims 1-8, 10, 13-17, and 19-21 as follows.

1. (Currently Amended) An apparatus ~~signal processor for Fast Fourier Transformation of M_R, $M_R > 1$, input data streams supplied in parallel~~, comprising:

a multiplexing device comprising M_R, $M_R \geq 1$, input terminals each receiving one of ~~the~~ M_R input data streams supplied in parallel, and an output terminal at which the M_R input data streams are output in a multiplexed manner;

a ~~Fast Fourier Transformation~~fast fourier transformation device configured to perform ~~Fast Fourier Transformation~~fast fourier transformation of a data stream supplied at an input terminal thereof and to output the fast fourier transformation~~Fast Fourier Transformation~~ transformed data stream at an output terminal thereof, the input terminal of the fast fourier transformation~~Fast Fourier Transformation~~ device being connected to the output terminal of the multiplexing device; and

a demultiplexing device comprising an input terminal connected to the output terminal of the fast fourier transformation~~Fast Fourier Transformation~~ device and M_R output terminals at which a respective one of M_R transformed output data streams is output in a demultiplexed manner,

wherein

each of the M_R input data streams contains a number of $N=2^k$ samples,

the fast fourier transformation~~Fast Fourier Transformation~~ device has a pipeline architecture composed of k stages with a respective feedback path including a single delay element per each stage of the pipeline architecture and is controlled by a first and second internal control signals,

the delay element in a feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline architecture imposes a delay of $M_R*N/2^i$ samples,

the first internal control signal is clocked M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied, and

the second internal control signals are clocked M_R times slower compared to the first internal control signal.

2. (Currently Amended) ~~A signal processor~~The apparatus according to claim 1, wherein

the multiplexing device is configured such that the M_R input data streams are multiplexed per data sample of the input data streams, and

the demultiplexing device is configured such that the transformed input data stream is demultiplexed per data sample of the transformed data stream.

3. (Currently Amended) ~~A signal processor~~The apparatus according to claim 2, wherein

a control signal supplied to the multiplexer and demultiplexer is clocked at a rate M_R times the clock rate of the supplied streams.

4. (Currently Amended) ~~A signal processor~~The apparatus according to claim 1, wherein the fast fourier transformation~~Fast Fourier Transformation~~ device has a ~~Radix-2 Single-path Delay Feedback~~radix-2 single-path delay feedback architecture.

5. (Currently Amended) ~~A signal processor~~The apparatus according to claim 4, wherein the pipeline architecture of the fast fourier transformation~~Fast Fourier Transformation~~ device is composed of ~~Butterfly~~ butterfly stages of types I and II.

6. (Currently Amended) ~~A signal processor~~The apparatus according to claim 5, wherein the first stage of the pipeline architecture receiving the multiplexed data streams is a ~~Butterfly~~ butterfly stage of type I for even and odd total numbers of k.

7. (Currently Amended) A network element comprising:

~~a signal processor according to claim 1~~a multiplexing device comprising M_R, $M_R \geq 1$, input terminals each receiving one of M_R input data streams supplied in parallel, and an output terminal at which the M_R input data streams are output in a multiplexed manner;

a fast fourier transformation device configured to perform fast fourier transformation of a data stream supplied at an input terminal thereof and to output the fast fourier transformation transformed data stream at an output terminal

thereof, the input terminal of the fast fourier transformation device being connected to the output terminal of the multiplexing device; and

a demultiplexing device comprising an input terminal connected to the output terminal of the fast fourier transformation device and M_R output terminals at which a respective one of M_R transformed output data streams is output in a demultiplexed manner,

wherein

each of the M_R input data streams contains a number of $N=2^k$ samples,

the fast fourier transformation device has a pipeline architecture composed of k stages with a respective feedback path including a single delay element per each stage of the pipeline architecture and is controlled by a first and second internal control signals,

the delay element in a feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline architecture imposes a delay of $M_R*N/2^i$ samples,

the first internal control signal is clocked M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied, and

the second internal control signals are clocked M_R times slower compared to the first internal control signal.

8. (Currently Amended) A terminal ~~configured to communicate via a communication network, the terminal~~ comprising: ~~a signal processor according to claim 1~~

a multiplexing device comprising M_R, $M_R > 1$, input terminals each receiving one of M_R input data streams supplied in parallel, and an output terminal at which the M_R input data streams are output in a multiplexed manner;

a fast fourier transformation device configured to perform fast fourier transformation of a data stream supplied at an input terminal thereof and to output the fast fourier transformation transformed data stream at an output terminal thereof, the input terminal of the fast fourier transformation device being connected to the output terminal of the multiplexing device; and

a demultiplexing device comprising an input terminal connected to the output terminal of the fast fourier transformation device and M_R output terminals at which a respective one of M_R transformed output data streams is output in a demultiplexed manner,

wherein

each of the M_R input data streams contains a number of $N=2^k$ samples,

the fast fourier transformation device has a pipeline architecture composed of k stages with a respective feedback path including a single delay element per each stage of the pipeline architecture and is controlled by a first and second internal control signals,

the delay element in a feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline architecture imposes a delay of $M_R*N/2^i$ samples,

the first internal control signal is clocked M_R times faster compared to a

clock rate at which the samples of the M_R streams are supplied, and

the second internal control signals are clocked M_R times slower compared to the first internal control signal.

9. (Canceled).

10. (Currently Amended) A ~~signal processing~~ method ~~for performing Fast Fourier Transformation of M_R, $M_R > 1$, input data streams supplied in parallel, the method~~ comprising:

multiplexing M_R, $M_R>1$, ~~the M_R~~ input data streams supplied in parallel to a multiplexed data stream;

performing ~~Fast Fourier Transformation~~fast fourier transformation of the multiplexed data stream and outputting the transformed data stream;

demultiplexing the transformed data stream to M_R transformed output data streams, wherein each of the M_R input data streams contains a number of $N=2^k$ samples;

performing fast fourier transformation~~Fast Fourier Transformation~~ using a pipeline of k stages with a respective feedback path imposing a delay on the samples per each stage of the pipeline;

controlling the performing of the fast fourier transformation~~Fast Fourier Transformation~~ by a first and second internal control signals and by imposing a delay of $M_R*N/2^i$ samples on the samples in the feedback path of an i^{th} stage, $1<=i<=k$, of the

pipeline;

clocking the first internal control signal M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied; and

clocking the second internal control signals M_R times slower compared to the first internal control signal.

11. (Previously Presented) A method according to claim 10, wherein

multiplexing is accomplished such that the M_R input data streams are multiplexed per data sample of the input data streams, and

demultiplexing is accomplished such that the transformed data stream is demultiplexed per data sample of the transformed data stream.

12. (Original) A method according to claim 11, wherein

clocking to the multiplexer and demultiplexer is performed at a rate M_R times the clock rate of the supplied streams.

13. (Currently Amended) A method according to claim 10, wherein

the fast fourier transformation~~Fast Fourier Transformation~~ processing is based on a ~~Radix-2~~radix-2 ~~Single-path Delay Feedback~~single-path delay feedback algorithm.

14. (Currently Amended)A method according to claim 13, wherein

the pipeline of processing stages for the fast fourier transformation~~Fast Fourier Transformation~~ is composed of ~~Butterfly~~ butterfly stages of types I and II .

15. (Currently Amended) A method according to claim 14, wherein

the first stage of the pipeline receiving the multiplexed data stream is a ~~Butterfly~~ butterfly stage of type I for even and odd total numbers of k.

16. (Currently Amended) A computer chip comprising: ~~at least a signal processor according to claim 1~~ a multiplexing device comprising M_R, $M_R > 1$, input terminals each receiving one of M_R input data streams supplied in parallel, and an output terminal at which the M_R input data streams are output in a multiplexed manner;

a fast fourier transformation device configured to perform fast fourier transformation of a data stream supplied at an input terminal thereof and to output the fast fourier transformation transformed data stream at an output terminal thereof, the input terminal of the fast fourier transformation device being connected to the output terminal of the multiplexing device; and

a demultiplexing device comprising an input terminal connected to the output terminal of the fast fourier transformation device and M_R output terminals at which a respective one of M_R transformed output data streams is output in a demultiplexed manner,

wherein

each of the M_R input data streams contains a number of $N=2^k$ samples,

the fast fourier transformation device has a pipeline architecture composed of k stages with a respective feedback path including a single delay element per each stage of the pipeline architecture and is controlled by a first and second internal control signals,

the delay element in a feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline architecture imposes a delay of $M_R*N/2^i$ samples,

the first internal control signal is clocked M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied, and

the second internal control signals are clocked M_R times slower compared to the first internal control signal.

17. (Currently Amended) A computer program, embodied on a machine-readable medium, said computer program ~~controlling a computer device to~~ configured to control a processor to perform a method comprising:

multiplexing M_R, $M_R>1$, ~~the M_R~~ input data streams supplied in parallel to a multiplexed data stream;

performing ~~Fast Fourier Transformation~~fast fourier transformation of the multiplexed data stream and outputting the transformed data stream;

demultiplexing the transformed data stream to M_R transformed output data streams, wherein each of the M_R input data streams contains a number of $N=2^k$ samples;

performing ~~Fast Fourier Transformation~~fast fourier transformation using a pipeline of k stages with a respective feedback path imposing a delay on the samples per each stage of the pipeline;

controlling the performing of the ~~Fast Fourier Transformation~~fast fourier transformation by a first and second internal control signals and by imposing a delay of $M_R*N/2^i$ samples on the samples in the feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline;

clocking the first internal control signal M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied; and

clocking the second internal control signals M_R times slower compared to the first internal control signal.

18. (Cancelled).

19. (Currently Amended) An apparatus ~~signal processor for Fast Fourier Transformation of M_R, $M_R>1$, input data streams supplied in parallel~~, comprising:

multiplexing means for multiplexing M_R, $M_R>1$, ~~the M_R~~ input data streams supplied in parallel to a multiplexed data stream;

first ~~Fast Fourier Transformation~~fast fourier transformation means for performing ~~Fast Fourier Transformation~~fast fourier transformation of the multiplexed data stream and outputting the transformed data stream;

demultiplexing means for demultiplexing the transformed data stream to M_R transformed output data streams, wherein each of the M_R input data streams contains a number of $N=2^k$ samples;

second ~~Fast Fourier Transformation~~fast fourier transformation means for performing fast fourier transformation~~Fast Fourier Transformation~~ using a pipeline of k stages with a respective feedback path imposing a delay on the samples per each stage of the pipeline;

controlling means for controlling the performing of the fast fourier transformation~~Fast Fourier Transformation~~ by a first and second internal control signals and by imposing a delay of $M_R*N/2^i$ samples on the samples in the feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline;

first clocking means for clocking the first internal control signal M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied; and

second clocking means for clocking the second internal control signals M_R times slower compared to the first internal control signal.

20. (Currently Amended) A system comprising:

a terminal configured to communicate via a communication network, the terminal comprising a signal processor configured for ~~Fast Fourier Transformation~~fast fourier transformation of M_R, $M_R>1$, input data streams supplied in parallel,

wherein the signal processor comprises

a multiplexing device comprising M_R input terminals each receiving one of the M_R input data streams, and an output terminal at which the M_R input data streams are output in a multiplexed manner;

a ~~Fast Fourier Transformation~~fast fourier transformation device configured to perform ~~Fast Fourier Transformation~~fast fourier transformation of a data stream supplied at an input terminal thereof and to output the ~~Fast Fourier Transformation~~fast fourier transformation transformed data stream at an output terminal thereof, the input terminal of the ~~Fast Fourier Transformation~~fast fourier transformation device being connected to the output terminal of the multiplexing device; and

a demultiplexing device comprising an input terminal connected to the output terminal of the ~~Fast Fourier Transformation~~fast fourier transformation device and M_R output terminals at which a respective one of M_R transformed output data streams is output in a demultiplexed manner, wherein

each of the M_R input data streams contains a number of $N=2^k$ samples,

the ~~Fast Fourier Transformation~~fast fourier transformation device has a pipeline architecture composed of k stages with a respective feedback path including a single delay element per each stage of the pipeline architecture and is controlled by a first and second internal control signals,

the delay element in a feedback path of an i^{th} stage, $1<=i<=k$, of the

pipeline architecture imposes a delay of $M_R*N/2^i$ samples,

the first internal control signal is clocked M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied, and

the second internal control signals are clocked M_R times slower compared to the first internal control signal.

21. (Currently Amended) A system comprising:

a network element, the network element comprising a signal processor configured for fast fourier transformation~~Fast Fourier Transformation~~ of M_R, $M_R>1$, input data streams supplied in parallel,

wherein the signal processor comprises

a multiplexing device comprising M_R input terminals each receiving one of the M_R input data streams, and an output terminal at which the M_R input data streams are output in a multiplexed manner;

a fast fourier transformation~~Fast Fourier Transformation~~ device configured to perform fast fourier transformation~~Fast Fourier Transformation~~ of a data stream supplied at an input terminal thereof and to output the fast fourier transformation~~Fast Fourier Transformation~~ transformed data stream at an output terminal thereof, the input terminal of the fast fourier transformation~~Fast Fourier Transformation~~ device being connected to the output terminal of the multiplexing device; and

a demultiplexing device comprising an input terminal connected to the output terminal of the fast fourier transformation~~Fast Fourier Transformation~~ device and M_R output terminals at which a respective one of M_R transformed output data streams is output in a demultiplexed manner, wherein

each of the M_R input data streams contains a number of $N=2^k$ samples,

the fast fourier transformation~~Fast Fourier Transformation~~ device has a pipeline architecture composed of k stages with a respective feedback path including a single delay element per each stage of the pipeline architecture and is controlled by a first and second internal control signals,

the delay element in a feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline architecture imposes a delay of $M_R*N/2^i$ samples,

the first internal control signal is clocked M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied, and

the second internal control signals are clocked M_R times slower compared to the first internal control signal.